TUSB6015 USB 2.0 High Speed Peripheral Controller Data Sheet

FEATURES

- USB 2.0 High-Speed (HS) Compliant Peripheral Controller Core
  - USB-IF TID # 40630005
- Integrated USB 2.0 PHY
- NOR FLASH - Like External Host Interface
- DP/DM lines are high impedance when the device is not powered
- Six physical endpoints
  - Each endpoint is configurable as IN or OUT with dedicated 1K buffer
- NOR Flash Interface Access modes:
  - Asynchronous 16-bit single access
  - Asynchronous 32-bit single access
  - Asynchronous 16x16 burst access w/ DMA
  - Synchronous 16x16 burst access with DMA (Max GPMC clock is 65 MHz)
- Interrupt on DP/DM line state change for CEA-936-A detect
- VBUS MAX Voltage rating will be 6V for USB Charging
- RoHS Complaint 80 Terminal BGA MICROSTAR JUNIOR Package

DESCRIPTION

The TUSB6015 is a USB 2.0 HS Peripheral Controller designed for seamless interface to an external Host processor through the NOR FLASH-like interface.

The NOR FLASH-like interface is a 16-bit, multiplexed address/data, interface with support for synchronous burst and single asynchronous read/write access. Configuration registers are accessible via the asynchronous chip select only; the End Point FIFO's are accessible via both the synchronous and asynchronous chip selects.

The device also has eight user configurable general purpose I/0 interface pins. The GPIO can be configured as an interrupt or wakeup source. Some GPIO have secondary NOR-flash DMA Request functionality.

The device is fully compliant with the Universal Serial Bus Specification Rev. 2.0.

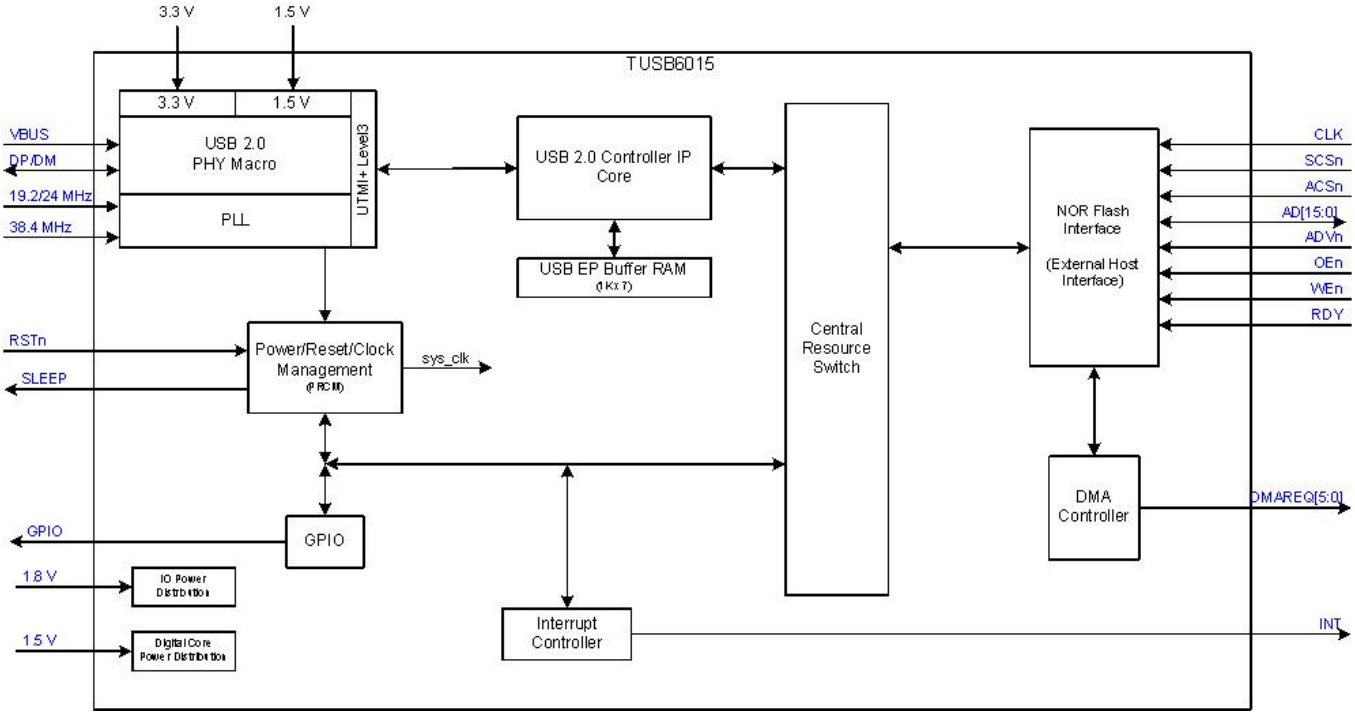
The ESD protection level is 2KV HBM (JESD22-A114D), 500V CDM (JESD22-C101C).

Ordering Information[1]

PACKAGED DEVICES	PACKAGE[2]	MARKING
TUSB6015IZQE	ZQE	TUSB6015I
TUSB6015IZQER•[3]	ZQE	TUSB6015I

[1] For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
[2] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
[3]The tape and reel option is available for TUSB6015IZQE by adding an R suffix.

Device Block Diagram



Electrical Characteristics

Absolute Maximum Ratings[1]

3.3V Supply Voltage, VDDA3P3 ..... -0.5 V to 4.2 V
1.8V Supply Voltage VDD18 ..... -0.5 V to 2.1 V
1.5V Supply Voltage, VDD15, VDDD1P5, VDDCM1P5, VDDA1P5 ..... -0.5 V to 2.1 V
USB VBUS Supply Voltage[2] ..... 0 V to 6.0 V
Input voltage, V_I, 3.3V USB[3] ..... -0.5 V to VDDA3P3 + 0.5 V
Output voltage, V_O, 3.3V USB ..... -0.5 V to VDDA3P3 + 0.5 V
Input clamp current, I_{IK} ..... ±20 mA
Output clamp current, I_{OK} ..... ±20 mA
Storage temperature range, Tstg ..... -65°C to 150°C

Recommended Operating Conditions

PARAMETER			MIN	TYP	MAX	UNIT
VDDA3P3	Supply voltage for PHY Analog		3	3.3	3.6	V
VDD18	Supply voltage for Digital I/O		1.62	1.8	1.98	V
VDD15 VDDD1P5 VDDCM1P5 VDDA1P5	Supply voltage for Digital Core Supply voltage for PHY Digital Supply voltage for PHY Common Module Supply voltage for PHY Analog		1.35	1.5	1.65	V
T_A	Operating Temperature	TUSB6015I (Industrial grade)	-40		85	°C

[1]Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

[2]VBUS can tolerate 6V for the lifetime of the device. It can handle 6.5V for 36 hours.

[3]TUSB6015 complies with short circuit withstand and AC stress conditions as described in Chapter 7.1.1 of the USB 2.0 specification.

Electrical Characteristics for the Digital I/O

T_A = -30°C - 85°C, V_{DD18} = 1.8 V ±10%, V_{SS} = 0 V (Unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
VI	Input voltage	LVCMOS		0		VDD18	V
V_O	Output voltage	LVCMOS		0		VDD18	V
V_{IH}	High–level input voltage	LVCMOS		0.7 x VDD18		VDD18	V
V_{IL}	Low–level input voltage	LVCMOS		0		0.3 x VDD18	V
V_{OH}	High–level output voltage	LVCMOS	I_{OH} = 8mA	0.8 × VDD18			V
V_{OL}	Low–level output voltage	LVCMOS open–drain	I_{OL} = 4mA			0.22 x VDD18	V
		LVCMOS	I_{OL} = 8mA			0.22 x VDD18	
		LVCMOS (1.5V_SWEN, 3.3V_SWEN only)	I_{OL} = 100uA		10		mV
I_{IH}	High–level input current	LVCMOS	$V_I = V_I$ max			±1	uA
I_{IL}	Low–level input current	LVCMOS	$V_I = V_I$ min			±1	uA
I_{OZ}	Output leakage current (high–Z)		$V_I = V_I$ max or V_{SS}			±20	uA
C_i	Input Capacitance (1.8V NOR Interface)					2.43	pF
t_r, t_f	Input rise/fall time			0		25	ns

Vbus - Electrical Characteristics for the Integrated USB 2.0 Transceiver, T_A = -30°C - 85°C,V_{DD15} = 1.5v±10%, V_{DD18} = 1.8V ±10%, V_{DDA1P5} = 1.5 V ±10%, V_{DDA3P3} = 3.3 ±10%,V_{DDD1P5} = 1.5 V ±10%, $V_{DDCM1P5}$ = 1.5 ±10%, V_{SS} = 0 V (unless otherwise noted)†

PARAMETER	MIN	TYP	MAX	UNIT
Input Levels				
Vbus Input Impedance	360		690	kΩ
Vbus Valid Comparator	4.4		4.75	V
Vbus leakage current (when device is powered off)			11	uA

†Characterization only. Limits approved by design.

DP and DM - Electrical Characteristics for the Integrated USB 2.0 Transceiver

T_A = -30°C - 85°C, V_{DD15} = 1.5v±10%, V_{DD18} = 1.8V±10%, V_{DDA1P5} = 1.5 V ±10%, V_{DDA3P3} = 3.3 ±10%, V_{DDD1P5} = 1.5, V ±10%, $V_{DDCM1P5}$ = 1.5±10%, V_{SS} = 0 V (unless otherwise noted)†

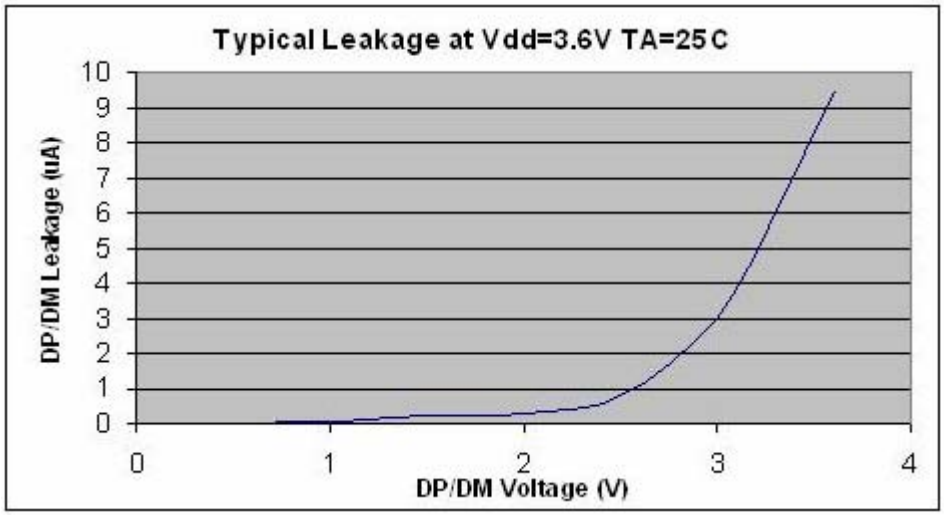
PARAMETER		MIN	TYP	MAX	UNIT
Input Levels for Full Speed					
V_{DI}	Full–speed differential input threshold	0.2			V
V_{CM}	Input (was differential) common mode range	0.8		2.5	V
Input Levels for High Speed					
V(HSSQ)	High–speed squelch detection threshold (differential signal amplitude)	100		150	mV
VDI	High–speed differential input threshold voltage	100			mV
CHSLOAD	Capacitance to ground on each line			5.5	pF
Output Levels for Full Speed					
VOL	Low–level output voltage	0		0.3	V
VOH	High–level output voltage (driven)	2.8		3.6	V
VO(SE1)	Output voltage on SE1	0.8			V
VO(CRS)	Output signal crossover voltage	1.3		2	V
Output Levels for High Speed					
V(HSOI)	High–speed idle level	-10		10	mV
V(HSOH)	High–speed data signaling high	360		440	mV
V(HSOL)	High–speed data signaling low	-10		10	mV
VID(CHIRPJ)	Chirp J level (differential voltage)	700		1100	mV
VID(CHIRPK)	Chirp K level (differential voltage)	-900		-500	mV
Driver Characteristics (Full Speed)					
tr	Full–speed rise time	4		20	ns
tf	Full–speed fall time	4		20	ns
t(RFM)	Full–speed rise/fall time matching	90%		110%	
Driver Characteristics (High Speed)					
tr	Rise time (10%-90%)	500			ps
tf	Fall time (10%-90%)	500			ps
ro(HSDRV)	Driver output resistance (serves as a high–speed termination)	40.5		49.5	Ω
t(FRFM)	Differential rise and fall time matching	90%		111.11%	
Clock Timings					
t(HSDRAT)	High–speed data rate	479.76		480.24	Mb/s
Single-Ended Receiver					
VIT+	Positive–going input threshold voltage			2.0	V
VIT-	Negative–going input threshold voltage	0.8			V
Vhys	Hysteresis voltage	200		500	mV

DP and DM - Electrical Characteristics for the Integrated USB 2.0 Transceiver (CONT'D)

INPUT LEAKAGE		TEST CONDITION	MIN	TYP	MAX	UNIT
DP/DM	Measurement taken with pull-up/dn disabled and device in idle mode	DP/DM Voltage = 0 – VDDA3.3	-1.3		1.3	uA
DP/DM	Measurement taken with pull-up/dn disabled and device in active mode	DP/DM Voltage = 2V		See Chart[1]	1.3	uA

†Characterization only. Limits approved by design.

[1]Typical DP/DM Input Leakage with pull-up/dn disabled and device in active mode



Power Sequencing Guidelines

Power-On Reset

The system reset function ensures an orderly start-up sequence for the TUSB6015. There is a one active low external system reset input (RSTn). The reset initializes the Power/Reset/Clock Manager (PRCM) module, which in turn generates all the internal resets to initialize USB 2.0 PHY Macro and synchronous logic in the core. While reset is asserted (active low), the dual functional pin is sampled to determine device configuration after reset.

Since TUSB6015 relies on a dual function pin to configure the device during reset, the reset must be sufficiently long for (external) marginal pull-up/pull-down to achieve the intended levels. Reset pulse duration should be at least three times actual RC constant time (with typical 22 kOhm marginal pull-up resistor with 50 pF load, reset pulse should be at least 3.3 µs).

All functional pins remain in same state even after RSTn is de-asserted and stay in that state until internal core reset is cleared. The internal core reset is held for 16 system clock cycles following low-to-high RSTn transition.

Upon power-on reset, the following must be determined for proper device initialization:

- System reference clock source

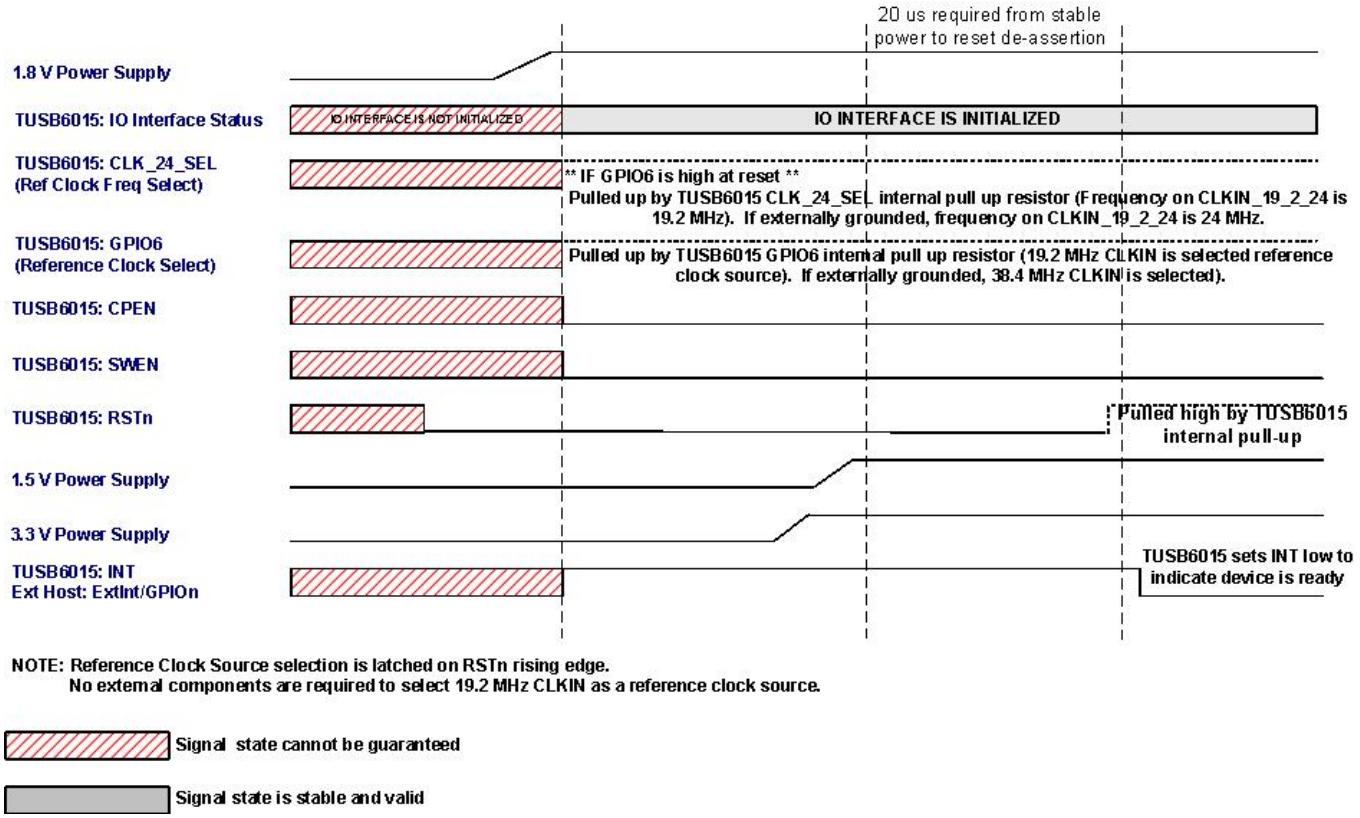
Device uses dual-mode pin to determine initial clock input setup. Dual function pin is latched during the reset. After the reset this terminal assumes the normal functionality.

External Pin	Function	Description
GPIO6	Reference Clock Frequency Select	Determines the reference clock pin 0 – 38.4 MHz (CLKIN_38_4 pin is used) 1 – 19.2 MHz (CLKIN_19_2_24 pin is used)
CLK_24_SEL	CLKIN_19_2_24 Frequency Select	Determines the reference frequency of the CLKIN_19_2_24 pin 0 – RSVD 1 – 19.2 MHz If GPIO6 is low at reset, this pin will have no effect on clock selection.

Upon exiting reset, the USB 2.0 PHY is not in the suspend state and the system clock (60 MHz) is enabled and free running. The USB 2.0 HS Peripheral Controller Core powers up and a session is not enabled. With session not enabled, all the USB 2.0 HS Peripheral Controller Core State Machine's are in the idle state.

After reset is de-asserted, the device asserts the DevReady interrupt to the External Host to indicate that it is ready to be programmed. The host reads the NOR Flash Interrupt Source register and decides how to proceed based on the device's current status.

System Power-Up Sequence



NOTE: Reference Clock Source selection is latched on RSTn rising edge.
No external components are required to select 19.2 MHz CLKIN as a reference clock source.

Signal state cannot be guaranteed

Signal state is stable and valid

Input Supply Current

T_A = 25°C

VDDA3.3 = 3.3V +/- 10%, VSS = 0V

PARAMETER		TEST CONDITIONS	TYP	UNIT
IDD	Input supply current	Idle[1]	16.5	uA
		No Bus Activity[2]	3.7	mA
		Active (Transmit / Receive)[3]	3.6	mA
		Reset[4]	2.7	mA

VDD1.8[7] = 1.8V +/- 10%, VSS = 0V

PARAMETER		TEST CONDITIONS	TYP	UNIT
IDD	Input supply current	Idle[1]	0.26	uA
		No Bus Activity[2]	157.0	uA
		Active (Transmit / Receive)[3]	350.0	uA
		Reset[4]	1.8	mA

Cumulative VDD1.5 = 1.5V +/- 10%, VSS = 0V
(VDD1.5, VDDD1.5, VDDCM1.5, VDDA1.5)

PARAMETER		TEST CONDITIONS	TYP	UNIT
IDD	Input supply current	Idle[1]	2.0	uA
		No Bus Activity[2]	56.5	mA
		Active (Transmit / Receive)[3]	58.0	mA
		Reset[4]	29.2	mA

[1] DevIdle bit set in Device PRCM Management Register, USB cable unplugged.
[2] Normal operation with no packets being transferred on the USB, except SOF every 125 µs.
[3] Bulk IN and OUT on one End Point. Packet size is 512 bytes.
[4] TUSB6015 RSTn asserted.

Input Clock Requirements

CLKIN 19.2 MHz Recommended Operating Conditions

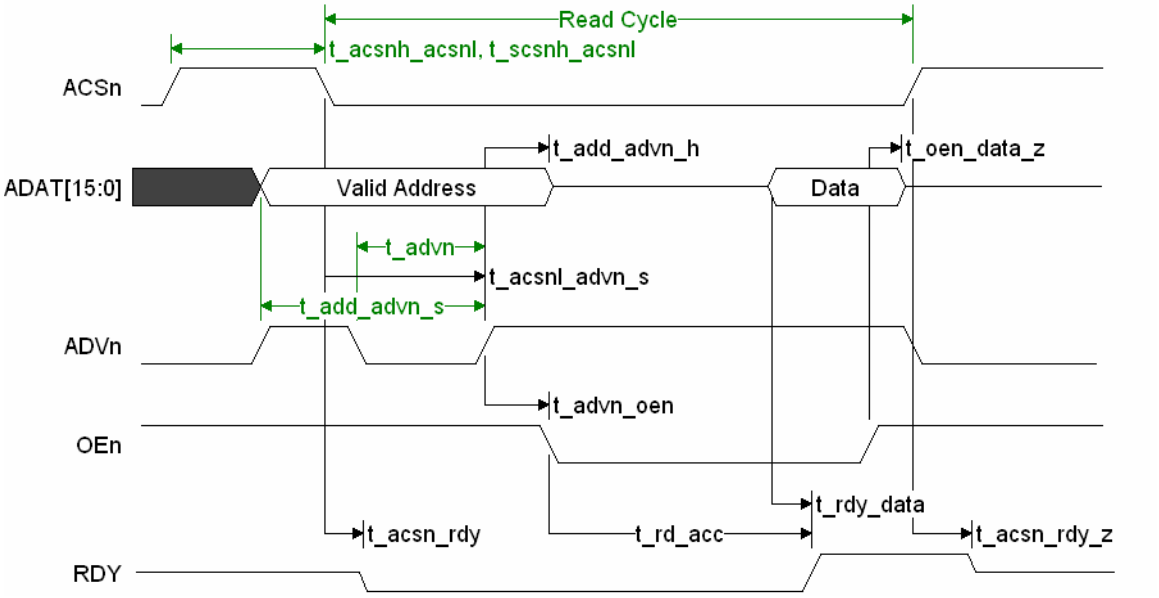
PARAMETER	VALUE
Nominal Clock Frequency (GPIO6 = high @ reset) (CLK_24_SEL = high @ reset)	19.20 MHz
Frequency Accuracy	+/- 100 ppm
Maximum Rise/Fall Time	5ns (10% to 90%)
Input Clock Type	Square Wave
Duty Cycle	45% - 55%
Input Capacitance Loading	4pF
Jitter	118 ps

CLKIN 38.4 MHz Recommended Operating Conditions

PARAMETER	VALUE
Nominal Clock Frequency (GPIO6 = low @ reset)	38.40 MHz
Frequency Accuracy	+/- 100 ppm
Input Clock Type	Sinusoid
Duty Cycle	45% - 55%
Input Common Mode Voltage VCM (V_{CM})	1 V +/- 100 mV
Vp-p	200 mV – 800 mV
Input Capacitance Loading	5 pF
Rin	180 kOhms
Jitter	100 ps (peak-to-peak)

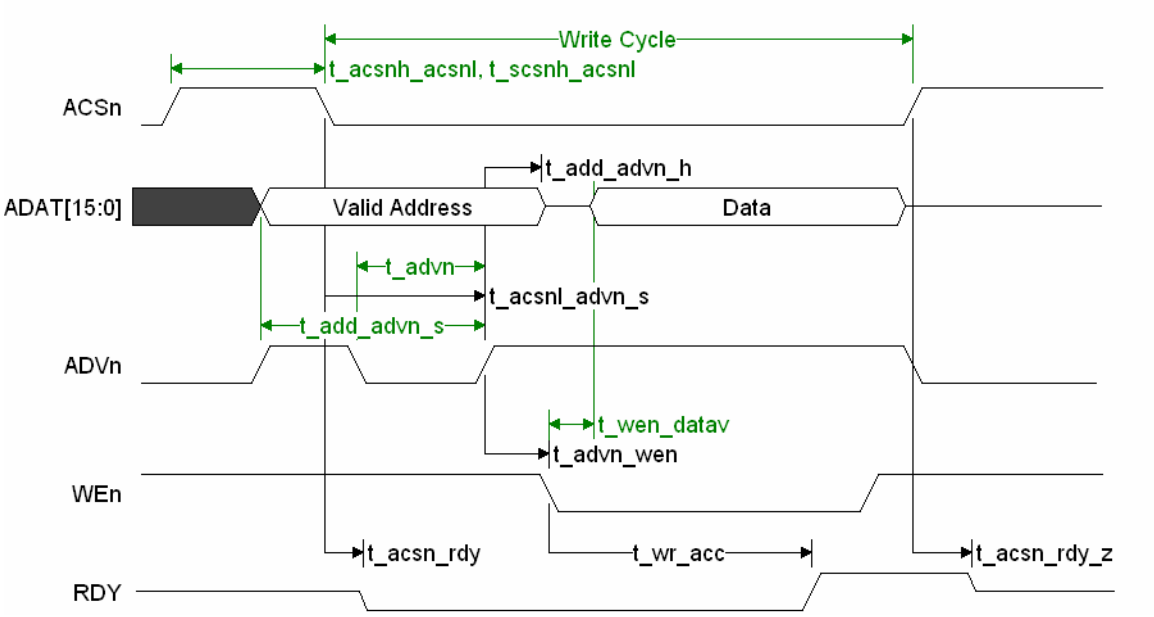
Timing Diagrams

Asynchronous Read Access



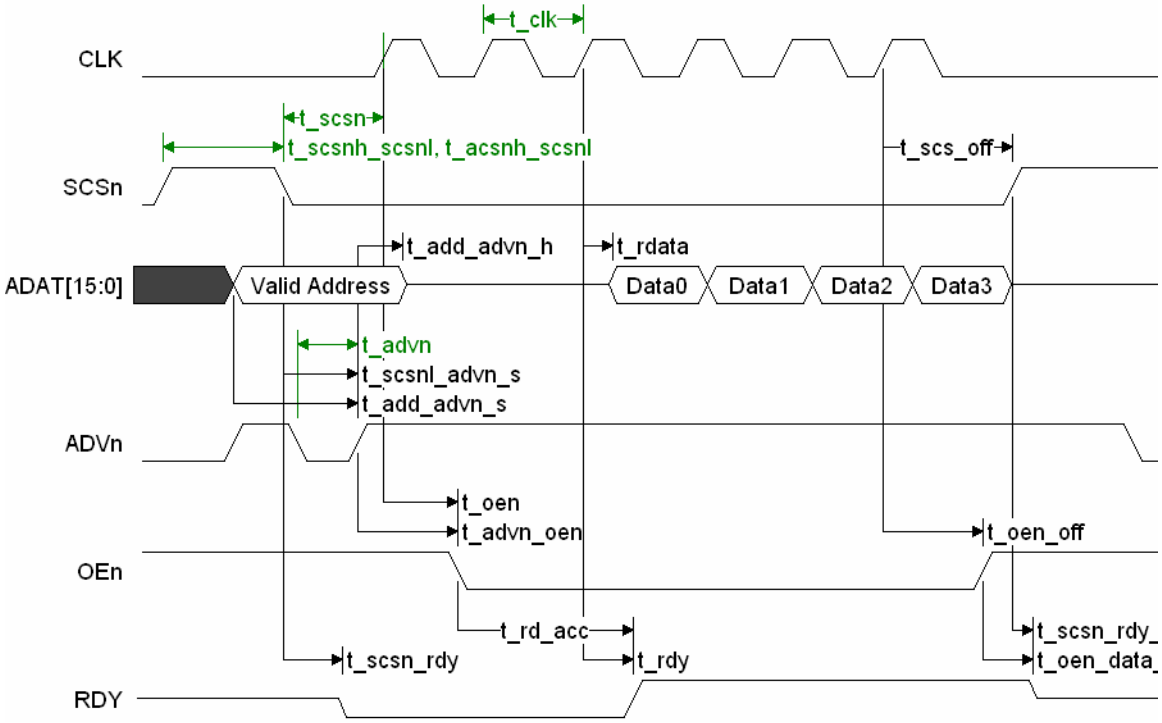
PARAMETER		MIN	MAX	UNIT
t_acsnh_acsnl	Delay time, ACSn high to ACSn low	8		ns
t_scsnh_acsnl	Delay time, SCSn high to ACSn low	8		ns
t_add_advn_h	Address Hold to ADVn high	0.8		ns
t_acsnl_advn_s	ACSn low Setup to ADVn high	18		ns
t_add_advn_s	Address Setup to ADVn high	18		ns
t_advn_oen	Sampled Address to OEn low	1		ns
t_advn	ADVn low pulse	7		ns
t_rd_acc	OEn low to RDY high (16-bit Register Access)	6	8	Sys Clk
	OEn low to RDY high (32-bit Register Access) 1st 16-bit	5	7	Sys Clk
	OEn low to RDY high (32-bit Register Access) 2nd 16-bit	2	4	Sys Clk
	OEn low to RDY high (FIFO Access, with DMAREQ) 1st 16-bit	3	4	Sys Clk
	OEn low to RDY high (FIFO Access, with DMAREQ) 2nd 16-bit	3	4	Sys Clk
t_acsn_rdy	ACSn low to RDY low		7	ns
t_acsn_rdy_z	ACSn high to RDY high-Z		7	ns
t_oen_data_z	OEn high to Data high-Z		8	ns
t_rdy_data	Delay time, RDY high to data valid	-1	6	ns

Asynchronous Write Access



PARAMETER		MIN	MAX	UNIT
t_acsnh_ascnl	Delay time, ACSn high to ACSn low	8		ns
t_scsnh_ascnl	Delay time, SCSn high to ACSn low	8		ns
t_add_advn_h	Address Hold to ADVn high	0.8		ns
t_acsnl_advn_s	ACSn low Setup to ADVn high	18		ns
t_add_advn_s	Address Setup to ADVn high	18		ns
t_advn	ADVn low pulse	7		ns
t_advn_wen	ADVn to WEn low	1		ns
t_wr_acc	WEn low to RDY high (16-bit Register Access)	3	5	Sys Clk
	WEn low to RDY high (32-bit Register Access) 1st 16-bit	2	4	Sys Clk
	WEn low to RDY high (32-bit Register Access) 2nd 16-bit	3	7	Sys Clk
	WEn low to RDY high (FIFO Access, with DMAREQ) 1st 16-bit	3	4	Sys Clk
	WEn low to RDY high (FIFO Access, with DMAREQ) 2nd 16-bit	3	4	Sys Clk
t_acsn_rdy	ACSn low to RDY low		7	ns
t_acsn_rdy_z	ACSn high to RDY high-Z		7	ns
t_wen_datav	Delay time, WEn low to Data valid		1-5ns	Sys Clk

Synchronous Burst Read Access

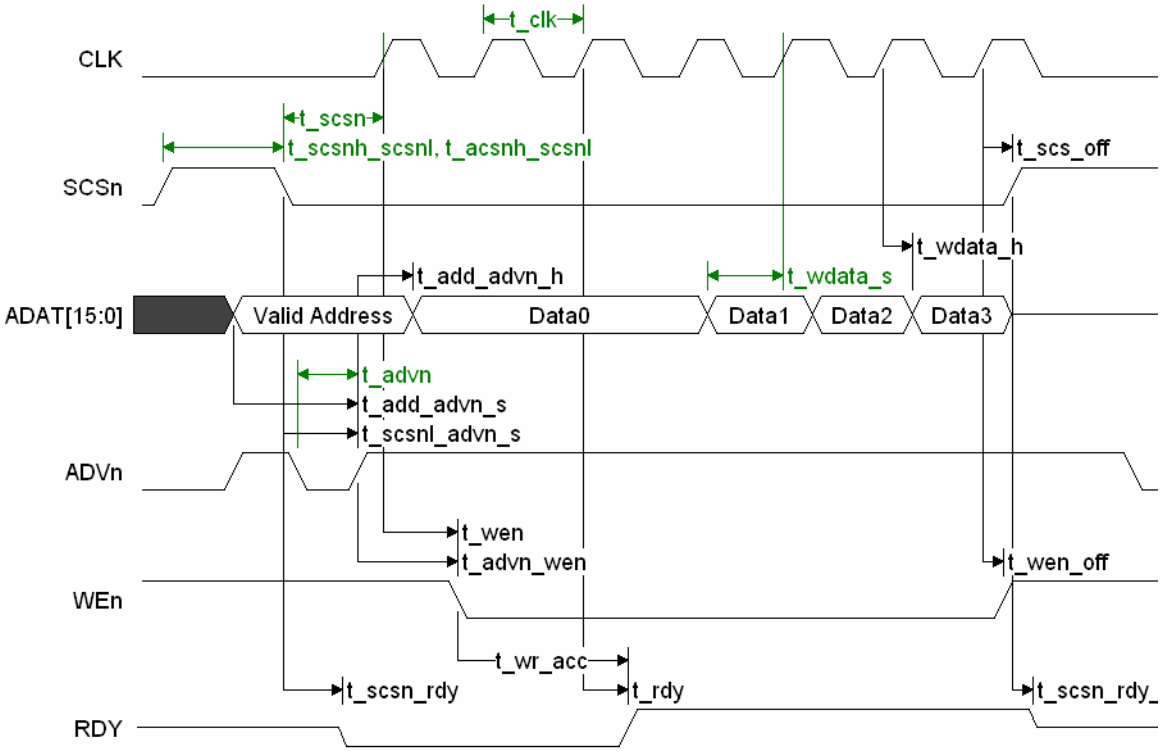


Notes: RDY going low is asynchronous to t_scsn_rdy. Going high, it is synchronous to CLK. Read Data output and RDY going high are synchronous to CLK. Valid Data Time programmable through Device Wait Count Register. Wait Count is not used for non-DMA synchronous reads.

PARAMETER		MIN	MAX	UNIT
t_clk	Cycle Time (max 67.5 MHz)	14.8		ns
t_scsnh_scsnl	Delay time, SCSn high to SCSn low	8		ns
t_acsnh_scsnl	Delay time, ACSn high to SCSn low	8		ns
t_scsn	Delay time, SCSn low to first rising edge of CLK	3ns	1+3ns	CLK
t_scs_off	CLK to SCSn high	4		ns
t_rdata	Read data output delay	2.2	9.2	ns
t_rdy	RDY output delay	2.2	8.2	Ns
t_advn	ADVn low pulse	7		Ns
t_advn_oen	ADVn high to OEn low	3		Ns
t_oen_off	CLK to OEn high	4		Ns
t_oen	OEn setup to CLK high	3.75		Ns
	OEn hold time	0		
t_rd_acc	Valid Data Time (with DMAREQ)	1[1]	32[2]	CLK
t_add_advn_h	Addr Hold time to ADVn high	0.8		Ns
t_scsnl_advn_s	SCSn low Setup to ADVn high	12		Ns
t_add_advn_s	Address Setup to ADVn high	12		Ns
t_scsn_rdy	SCSn low to RDY valid low		7	ns
t_scsn_rdy_z	SCSn high to RDY high-Z		7	ns
t_oen_data_z	OEn high to Data high-Z		8	ns

[1]Device Wait Count Register = 0 or 1.
[2]Device Wait Count Register = 31.

Synchronous Burst Write Access



Note: RDY going low is asynchronous to t_scsn_rdy. Going high, it is synchronous to CLK. Valid Data Time programmable through Device Wait Count Register. For Wait Count values other than 0 or 1 (when DMAREQ is used), t_wr_acc = Wait Count + 1.

PARAMETER		MIN	MAX	UNIT
t_clk	Cycle Time (max 67.5 MHz)	14.8		ns
t_scsnh_scsnl	Delay time, SCSn high to SCSn low	8		ns
t_acsnh_scsnl	Delay time, ACSn high to SCSn low	8		ns
t_scsn	Delay time, SCSn low to first rising edge of CLK	3ns	1+3ns	CLK
t_scs_off	CLK to SCSn high	1+3ns		Sys Clk
t_wdata_s	Data setup to CLK high	3.75		ns
t_wdata_h	Data hold time	0.6		ns
t_rdy	CLK to RDY output delay	2.2	8.2	ns
t_add_advn_h	Address Hold	0.8		ns
t_scsnl_advn_s	SCSn low Setup to ADVn high	12		ns
t_add_advn_s	Address Setup to ADVn high	12		ns
t_advn	ADVn low pulse	7		ns
t_advn_wen	ADVn high to WEn low	1+3ns		CLK
t_wen_off	CLK to WEn high	1+3ns		Sys Clk
t_wen	WEn setup to CLK high	3.75		ns
	WEn hold time	0		
t_wr_acc	Valid Data Time (with DMAREQ)	1[1]	32[2]	CLK
t_scsn_rdy	SCSn low to RDY valid low		7	ns
t_scsn_rdy_z	SCSn high to RDY high-Z		7	ns

[1]Device Wait Count Register = 0 or 1.
[2]Device Wait Count Register = 31.

Pin Descriptions

TERMINAL		TYPE	I/O	RESET STATE	DESCRIPTION
NAME	BALL				
VDD15	A1	Supply	-	-	Digital core power supply, 1.5 V
VSS	A2	Supply	-	-	Ground
CLK_24_SEL	A3	LVCMOS Failsafe[1]	I	In with Pull-up	CLKIN_19_2_24 Frequency Select at Reset CLK 24 SEL = HIGH, 19.2 MHz CLK 24 SEL = LOW, RSVD If GPIO6 is low at reset, this pin will have no effect on clock selection.
CLKIN_38_4	A4	LVCMOS Failsafe[1]	I	In	System Clock In. Connect directly to ground if not used.
CLKIN_19_2_24	A5	LVCMOS Failsafe[1]	I	In	System Clock In. Connect directly to ground if not used.
VSS	A6	Supply	-	-	Ground
VDD18	A7	Supply	-	-	IO Power Supply, 1.8 V
OEn	A8	LVCMOS Failsafe[1]	I	In with Pull-up	Output Enable
VDD15	A9	Supply	-	-	Digital core power supply, 1.5 V
VSSREF	B1	Supply	-	-	Ground reference for the reference circuits
GPIO7	B2	LVCMOS Failsafe[1]	I/O	In with Pull-up	GPIO 7
VDD15	B3	Supply	-	-	Digital core power supply, 1.5 V
VSS	B4	Supply	-	-	Ground
VDD18	B5	Supply	-	-	IO Power Supply, 1.8 V
GPIO2_DMAREQ2	B6	LVCMOS Failsafe[1]	I/O	In with Pull-up	GPIO 2 / DMA Request 2
ADAT15	B7	LVCMOS	I/O	In with Pull-up	Multiplexed ADDRESS.15/DATA.14
ADAT16	B8	LVCMOS	I/O	In with Pull-up	Multiplexed ADDRESS.16/DATA.15
VSS	B9	Supply	-	-	Ground
VDDA3P3	C1	Supply	-	-	3.3V Analog Supply
R1	C2	Bias	I	-	High precision external resistor used for calibration. (R1 value: 10.7 K +/- 1%)
GPIO4_DMAREQ4	C4	LVCMOS Failsafe[1]	I/O	In with Pull-up	GPIO 4 / DMA Request 4
VDD15	C5	Supply	-	-	Digital core power supply, 1.5 V
ADVn	C6	LVCMOS Failsafe[1]	I	In with Pull-up	Address Valid
ADAT12	C7	LVCMOS Failsafe[1]	I/O	In with Pull-up	Multiplexed ADDRESS.12/DATA.11
ADAT14	C8	LVCMOS Failsafe[1]	I/O	In with Pull-up	Multiplexed ADDRESS.14/DATA.13

CLK	C9	LVCMOS Failsafe[1]	I	In with Pull-up	NOR Interface Clock
DP	D1	USB	I/O	-	USB Differential Pair
VDDCM1P5	D2	Supply	-	-	1.5V PLL Supply
VSSCM1P5	D3	Supply	-	-	1.5V PLL Ground
TEST	D4	LVCMOS	I	-	Test Mode. Under normal operation this signal should be tied directly to GND.
GPIO1	D5	LVCMOS Failsafe[1]	I/O	In with Pull-up	GPIO 1
WEn	D6	LVCMOS Failsafe[1]	I	In with Pull-up	Write Enable
ADAT13	D7	LVCMOS Failsafe[1]	I/O	In with Pull-up	Multiplexed ADDRESS.13/DATA.12
ADAT11	D8	LVCMOS Failsafe[1]	I/O	In with Pull-up	Multiplexed ADDRESS.11/DATA.10
VDD15	D9	Supply	-	-	Digital core power supply, 1.5 V
VSSA1P5	E1	Supply	-	-	1.5V Analog Ground
DM	E2	USB	I/O	-	USB Differential Pair
VDDA1P5	E3	Supply	-	-	1.5V Analog Supply
VSSA3P3	E4	Supply	-	-	3.3V Analog Ground
VSS	E5	Supply	-	-	Ground
ADAT2	E6	LVCMOS Failsafe[1]	I/O	In with Pull-up	Multiplexed ADDRESS.2/DATA.1
GPIO5_DMAREQ5	E7	LVCMOS Failsafe[1]	I/O	In with Pull-up	GPIO 5 / DMA Request 5
GPIO3_DMAREQ3	E8	LVCMOS Failsafe[1]	I/O	In with Pull-up	GPIO 3 / DMA Request 3
VSS	E9	Supply	-	-	Ground
VDDD1P5	F1	Supply	-	-	1.5V Digital Supply
ID	F2	USB	I	-	Should be left floating as a USB device.
VBUS	F3	USB	I	-	USB VBUS
VSSD1P5	F4	Supply	-	-	1.5V Digital Ground
GPIO6	F5	LVCMOS Failsafe[1]	I/O	In with Pull-up	GPIO 6 / Input Clock Source Select at reset. GPIO6 = HIGH, 19.2/24 MHz GPIO6 = LOW, 38.4 MHz
ADAT1	F6	LVCMOS Failsafe[1]	I/O	In with Pull-up	Multiplexed ADDRESS.1/DATA.0
ADAT10	F7	LVCMOS Failsafe[1]	I/O	In with Pull-up	Multiplexed ADDRESS.10/DATA.9
ADAT9	F8	LVCMOS Failsafe[1]	I/O	In with Pull-up	Multiplexed ADDRESS.9/DATA.8
VDD15	F9	Supply	-	In with Pull-up	Digital core power supply, 1.5 V
VSS	G1	Supply	-	-	Ground
1.5V_SWEN	G2	LVCMOS	O	0	Switch Enable for 1.5V supply for Vbat/Vbus

		Failsafe[1]			Switch, if applicable
3.3V_SWEN	G3	LVCMOS Failsafe[1]	O	0	Switch Enable for 3.3V supply for Vbat/Vbus Switch, if applicable
ACSn	G4	LVCMOS Failsafe[1]	I	In with Pull-up	Asynchronous Chip Select
ADAT3	G5	LVCMOS Failsafe[1]	I/O	In with Pull-up	Multiplexed ADDRESS.3/DATA.2
ADAT4	G6	LVCMOS Failsafe[1]	I/O	In with Pull-up	Multiplexed ADDRESS.4/DATA.3
RDY	G7	LVCMOS tri-state	O	high z	Ready
SCSn	G8	LVCMOS	I	In with Pull-up	Synchronous Chip Select
VSS	G9	Supply	-	-	Ground
RSTn	H1	LVCMOS Failsafe[1]	I	In with Pull-up	Reset Active Low
CPEN	H2	LVCMOS Failsafe[1]	O	0	5V Charge Pump Enable, if applicable
SLEEP	H3	LVCMOS Failsafe[1]	O	0	Use for external power supply low power mode when idle, if applicable
GPIO0	H4	LVCMOS Failsafe[1]	I/O	In with Pull-up	GPIO 0
ADAT5	H5	LVCMOS Failsafe[1]	I/O	In with Pull-up	Multiplexed ADDRESS.5/DATA.4
ADAT6	H6	LVCMOS Failsafe[1]	I/O	In with Pull-up	Multiplexed ADDRESS.6/DATA.5
ADAT7	H7	LVCMOS Failsafe[1]	I/O	In with Pull-up	Multiplexed ADDRESS.7/DATA.6
ADAT8	H8	LVCMOS Failsafe[1]	I/O	In with Pull-up	Multiplexed ADDRESS.8/DATA.7
VDD18	H9	Supply	-	-	IO Power Supply, 1.8 V
VDD18	J1	Supply	-	-	IO Power Supply, 1.8 V
VSS	J2	Supply	-	-	Ground
VDD15	J3	Supply	-	-	Digital core power supply, 1.5 V
VSS	J4	Supply	-	-	Ground
DMAREQ1	J5	LVCMOS Failsafe[1]	O	1	DMA Request 1
VDD18	J6	Supply	-	-	IO Power Supply, 1.8 V
DMAREQ0	J7	LVCMOS Failsafe[1]	O	1	DMA Request 0
VSS	J8	Supply	-	-	Ground
INT	J9	LVCMOS Failsafe[1]	O	1	Interrupt

[1]Failsafe means that the signal can toggle when VDD18 is not present without damaging the device.

External Components

USB PHY Voltage and Current Bias Resistor Pin: R1

This signal must connect to a precision external resistance to set the internal operating reference currents and cable driver output currents. A resistance of 10.7 k• ± 1% (temperature coefficient ±100ppm/°C) is necessary to meet requirements set forth in the Universal Serial Bus Revision 2.0 specification.

The side of the resistor not connected to the R1 signal should connect through a low impedance path to the circuit board ground plane.

USB PHY Voltage and Current Reference Ground: VSSREF

This signal is the reference ground for the voltage and current reference circuitry internal to the Data/Port macro. This signal must connect to the low impedance circuit board ground plane.

USB PHY Power Connections: VDDCM1P5, VDDA1P5, VDDD1P5, VDDA3P3

Decoupling capacitors are required to suppress high-frequency switching noise and stabilize the supply voltage. A decoupling capacitor is most effective when it is close to the chip. This minimizes the inductance of the circuit board wiring and interconnects.

The USB 2.0 PHY Macro has two power rails, 1.5V (VDDCM1P5, VDDD1P5, VDDA1P5) and 3.3V (VDDA3P3). Each power connection has its own associated ground connection, 1.5V (VSSCM1P5, VSSD1P5, VSSA1P5) and 3.3V (VSSA3P3). Each supply is isolated from the others to provide noise isolation.

A combination of high-frequency capacitors near each terminal is suggested, such as paralleled 1uF, 0.01uF, and 0.001uF capacitors. A lower frequency 10uF filter capacitor is also recommended. A series inductor on the analog supplies is also recommended. All ground pins must connect through a low impedance path to the circuit board ground plane. All grounds can be connected to each other.

- VDDCM1P5 (Common Module 1.5V Supply) - (1) 1µf , (1) 0.1µf, 0.01µf, (1) 0.001µf, (1) 10µf
- VSSCM1P5 (Common Module Ground)
- VDDD1P5 (Digital 1.5V Supply) - (1) 0.1µf, (1) 0.001µf, (1) 10µf
- VSSD1P5 (Digital 1.5V Ground)
- VDDA1P5 (Analog 1.5V Supply) - (1) 0.1µf, (1) 0.001µf, (1) 10µf, with a series inductor between the main supply and the device, the caps between the inductor and the device.
- VSSA1P5 (Analog 1.5V Ground)
- VDDA3P3 (Analog 3.3V Supply) - (1) 0.1µf, (1) 0.001µf, (1) 10µf, with a series inductor between the main supply and the device, the caps between the inductor and the device.
- VDDA3P3 (Analog 3.3V Ground)

Digital Power Connections: VDD18, VDD15

The digital portion of the TUSB6015 has two power rails, 1.5V (VDD15) and 1.8V (VDD18). There is one digital ground connection (VSS). Each supply is isolated from the others to provide noise isolation.

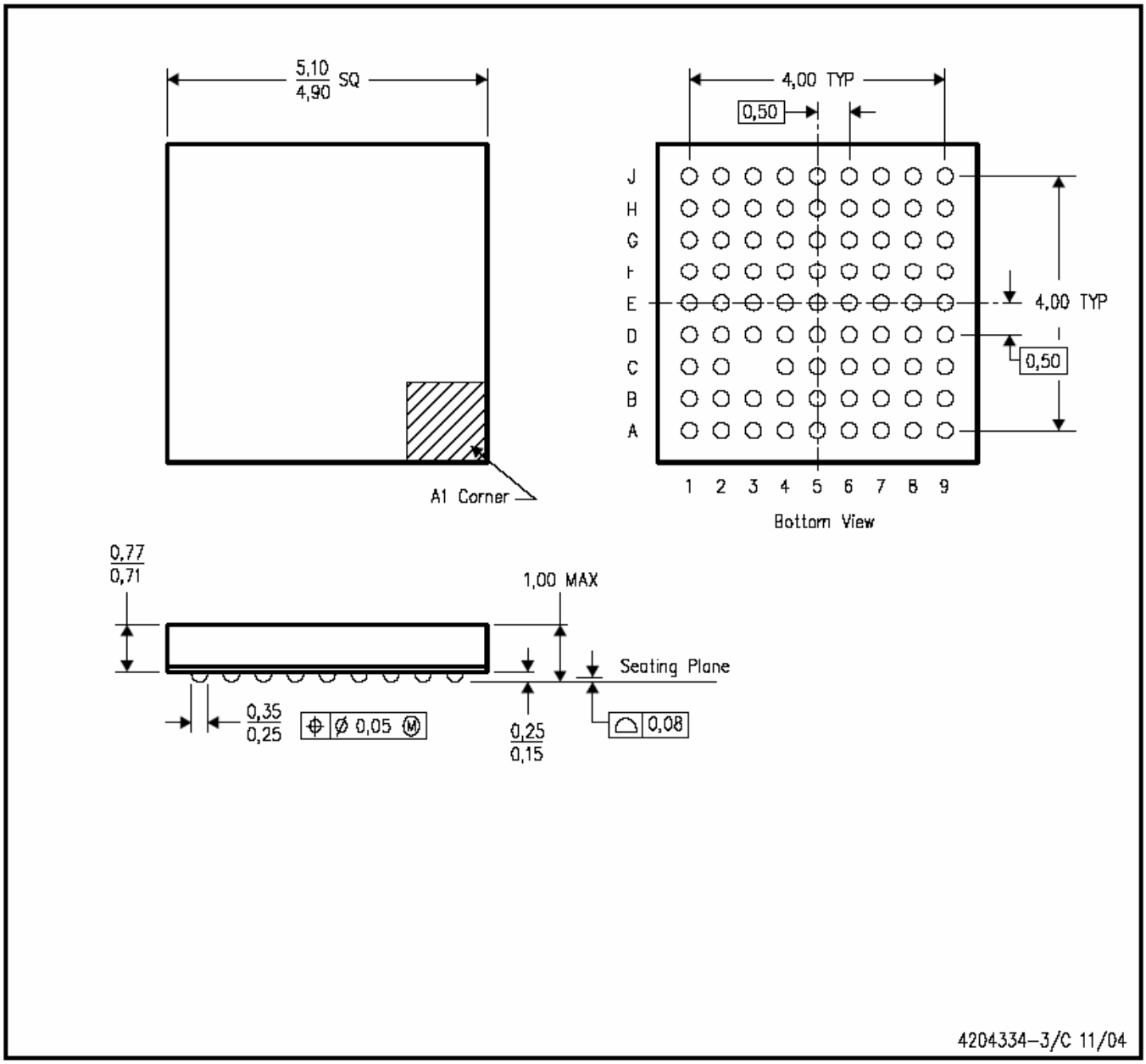
A combination of high-frequency capacitors near each terminal is suggested, such as paralleled 0.01uF and 0.001uF capacitors. A lower frequency 10uF filter capacitor is also recommended. All ground pins must connect through a low impedance path to the circuit board ground plane. All grounds can be connected to each other.

- VDD15 (Digital Core Voltage 1.5V Supply) - (5) 0.1µf, (5) 0.001µf, (1) 10µf
- VDD18 (Digital IO Voltage 1.8V Supply) - (5) 0.1µf, (5) 0.001µf, (1) 10µf
- VSS (Digital Ground)

Mechanical Characteristics

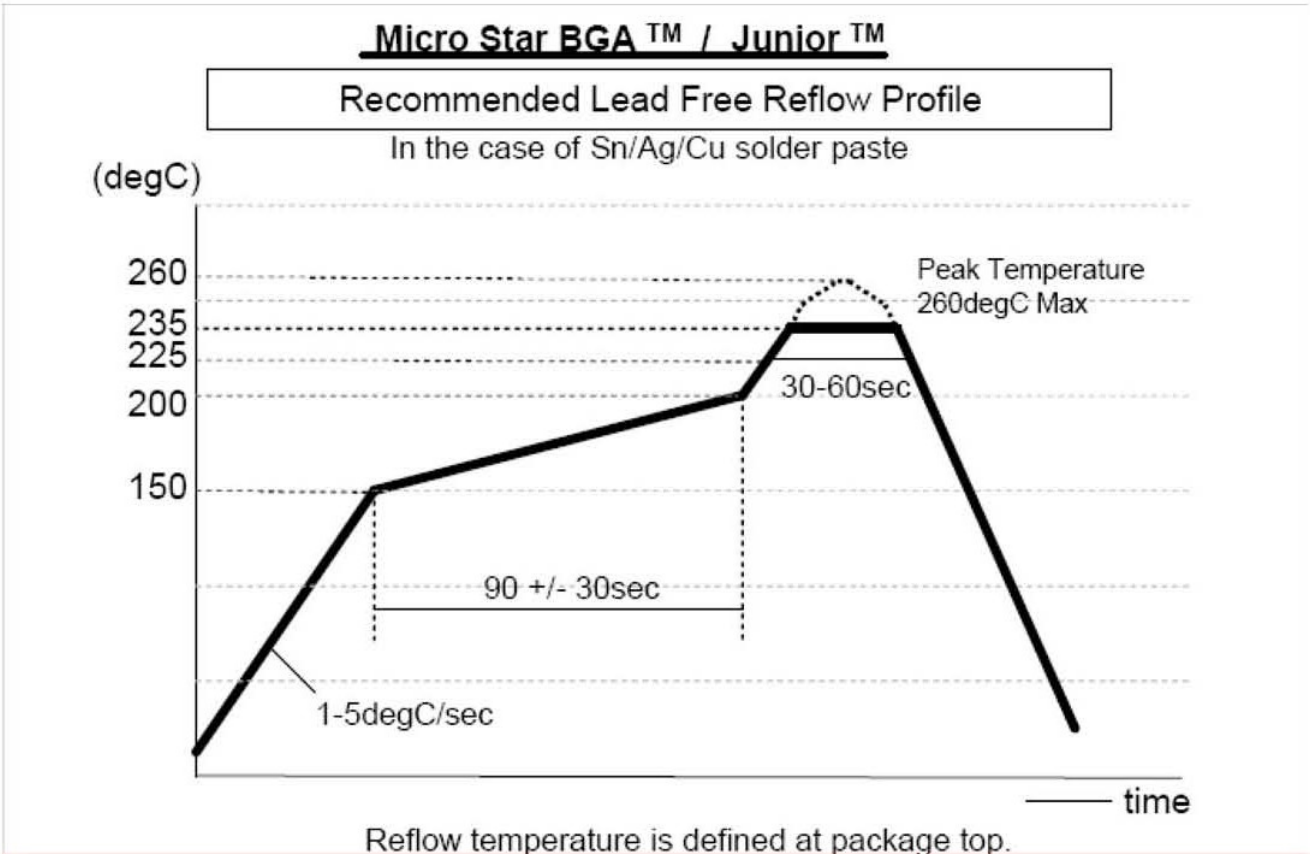
TUSB6015 uses an 80-pin u*BGA package. The lead-free solder ball composition is Sn/Ag1.2Cu0.5 The substrate plating on the die side where the die bonds to is NiAu, The substrate finish on the bottom side where the solder balls attach to is bare Cu.

ZQE (S-PBGA-N80) Plastic Ball Grid Array



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-225
D. This package is lead-free.

Reflow Conditions



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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TUSB6015IZQE	ACTIVE	BGA MICROSTAR JUNIOR	ZQE	80	360	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR
TUSB6015IZQER	ACTIVE	BGA MICROSTAR JUNIOR	ZQE	80	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR

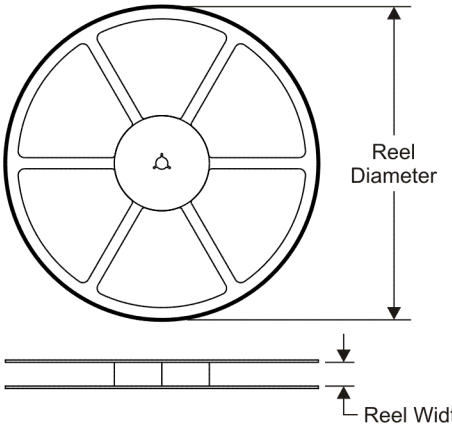
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

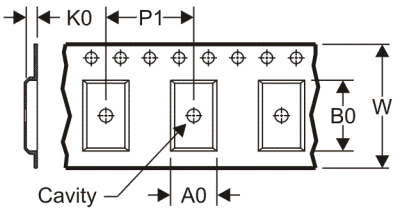
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

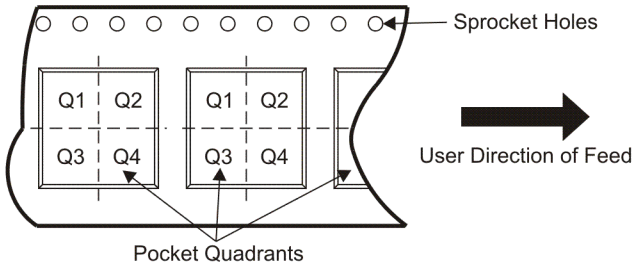


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

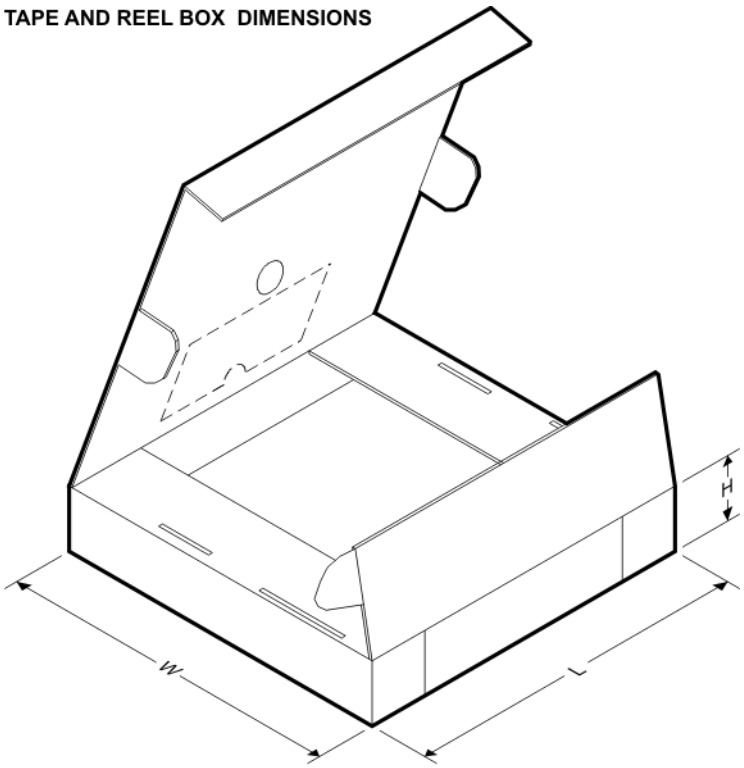
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB6015IZQER	BGA MICROSTAR JUNIOR	ZQE	80	2500	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q1

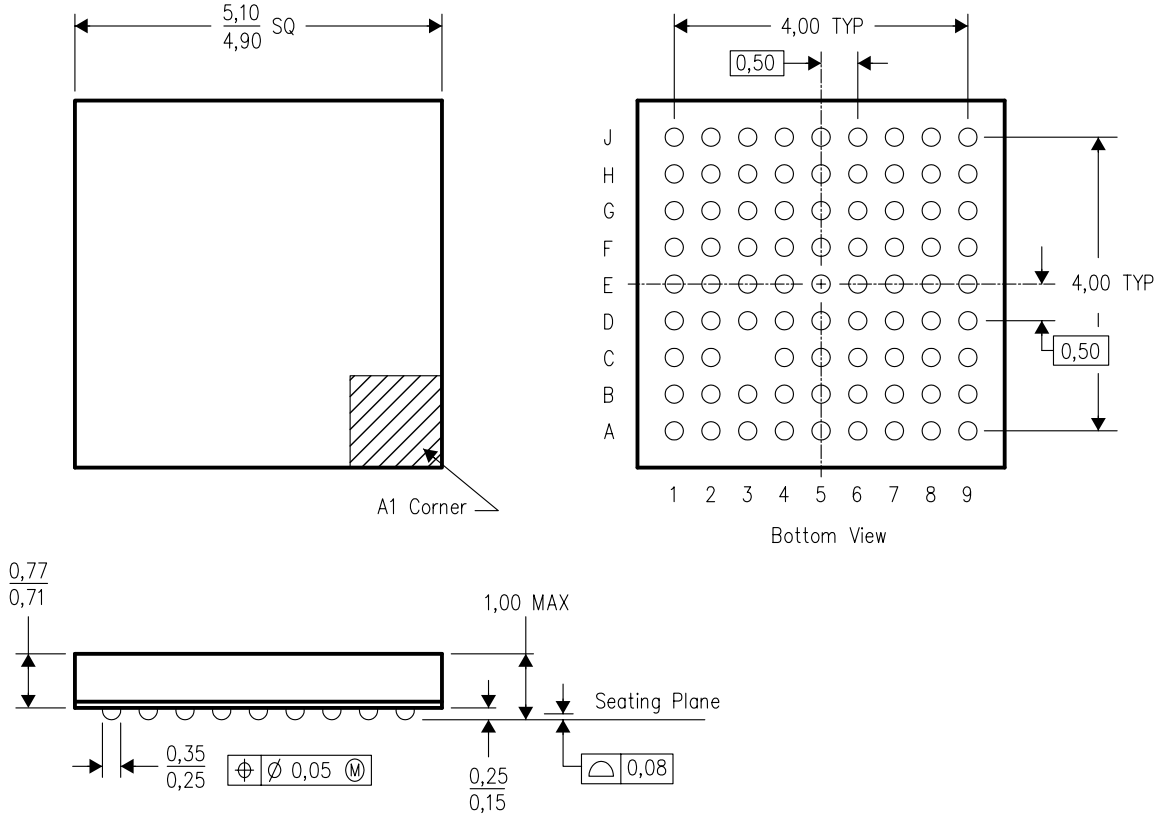
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB6015IZQER	BGA MICROSTAR JUNIOR	ZQE	80	2500	340.5	333.0	20.6

ZQE (S–PBGA–N80) PLASTIC BALL GRID ARRAY



4204334–4/D 10/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225
D. This is a lead–free solder ball design.

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